UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/761,204	01/22/2004	Noriaki Oda	8017-1122	2345

466 7590 04/10/2006

YOUNG & THOMPSON
745 SOUTH 23RD STREET
2ND FLOOR
ARLINGTON, VA 22202

EXAMINER	
WILLIAMS, ALEXANDER O	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 04/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/761,204	ODA, NORIAKI
	Examiner	Art Unit
	Alexander O. Williams	2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1, 3 to 11, 14 and 42 to 49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3 to 11, 14 and 42 to 49* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/22/04 & 3/14/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 10/761204 Attorney's Docket #: 8017-1122
Filing Date: 1/22/2004; claimed foreign priority to 1/30/2003

Applicant: Oda Examiner: Alexander Williams

Applicant's Amendment filed 1/31/06 to the election of the species of figure 2 (claims 1 to 11, 14 and 42 to 49), filed 8/30/05, has been acknowledged.

Claims 2, 12, 13 and 15 to 41 have been cancelled.

Claims 1, 2 to 11, 14 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, it is unclear and confusing to what is meant by "a lower copper layer that is formed closer to said semiconductor substrate than said upper copper layer; wherein a copper area ratio of said lower copper layer under said bonding pads is equal to or lower than that of said upper copper layer." Applicant claims "bonding pads" and "a copper area ratio of the said lower copper layer under said bonding pads is equal to or lower than that of said upper copper layer." How do you determine the area of copper layer under bonding pads when one ad is shown?

Any of claims 1, 2 to 11, 14 not specifically addressed above are rejected as being dependent on one or more of the claims which have been specifically objected to above.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3 to 11, 14 and 42 to 49, insofar as they can be understood, are rejected under 35 U.S.C. § 102(e) as being anticipated by Ker et al. (U.S. Patent Application Publication # 2001/0010408 A1).

1. Ker et al. (figures 1 to 23) specifically figure 5 show a semiconductor device, comprising: bonding pads **250** that are formed on a semiconductor substrate **200**; an upper copper layer **240** that is formed on the lower surface of said bonding pads with a barrier metal interposed; and a lower copper layer **210** that is formed closer to said semiconductor substrate than said upper copper layer; wherein a copper area ratio of said lower copper layer under said bonding pads is equal to or lower than that of said upper copper layer, and wherein said lower copper

layer is not electrically connected to said upper copper layer under said bonding pads.

3. A semiconductor device according to claim 1, Ker et al. show wherein the copper area ratio of said upper copper layer is greater than that of other copper layers that are formed as circuit interconnects on said semiconductor substrate.

4. A semiconductor device according to claim 1, Ker et al. show wherein the copper area ratio of said upper copper layer is at least 70%.

5. A semiconductor device according to claim 1, Ker et al. show wherein the planar dimensions of said bonding pads and said upper copper layer are substantially equal.

6. A semiconductor device according to claim 1, Ker et al. show wherein said upper copper layer is constituted by a plurality of copper layers.

7. A semiconductor device according to claim 6, Ker et al. show wherein the copper area ratios of each copper layer of said upper copper layer are substantially the same.

8. A semiconductor device according to claim 6, Ker et al. further comprising: interlevel dielectric films that are provided between each of the copper layers of said upper copper layer; and via-plugs composed of copper that are embedded in said interlevel dielectric films wherein each of the copper layers of said upper copper layer are connected by way of said via-plugs.

9. A semiconductor device according to claim 8, Ker et al. show wherein the copper layer pattern of the copper layer that is positioned uppermost in said upper copper layer and said via-plugs that are connected to the copper layer pattern are embedded in a dielectric film that is composed of a first material.

10. A semiconductor device according to claim 1, Ker et al. show wherein the copper area ratio of said lower copper layer is at least 15% and not greater than 95%.

11. A semiconductor device according to claim 1, Ker et al. show wherein said lower copper layer is constituted by a plurality of copper layers.

14. A semiconductor device according to claim 13, Ker et al. show wherein each of the copper layers of said lower copper layer are constituted by a copper pattern that is embedded in a dielectric film that is composed of a second material having a lower relative dielectric constant than said first material.

42. Ker et al. (figures 1 to 23) specifically figure 23 show a semiconductor device comprising: a bonding region in which a bonding pad **56** is formed; an internal circuit region provided inside of said bonding region, said internal circuit region having a multilevel wiring structure that includes a plurality of copper interconnect layers **55,54,53** at a first level and a plurality of copper interconnect layers **51,52** at second level; and

a copper layer **55** formed in said bonding region under said bonding pad in electrical contact therewith, one of said copper

interconnect layers at said first level being elongated from said internal circuit region to said bonding region under said copper layer in electrical isolation therefrom.

43. The device as claimed in claim 42, Ker et al. show wherein one of said copper interconnect layers at said second level is further elongated from said internal circuit region to said bonding region under said copper layer in electrical isolation from said copper layer and from one of said copper interconnect layers at said first level.

44. The device as claimed in claim 42, Ker et al. show wherein said copper layer includes first and second copper layers and a via-plug sandwiched therebetween.

45. The device as claimed in claim 44, Ker et al. show wherein said multilevel wiring structure further includes a plurality of copper interconnect layers at a third level and a plurality of copper interconnect layers at a fourth level, said first copper layer being formed at said third level and said second copper layer being formed at said fourth level.

46. The device as claimed in claim 45, Ker et al. show wherein said bonding pad is in electrical contact with said second copper layer, and one of said copper interconnect layers at said fourth level has an electrical contact with said second copper layer.

Response

Applicant's arguments filed 1/31/06 have been fully considered, but are moot in view of the new grounds of rejections detailed above.

The listed references are cited as of interest to this application, but not applied at time.

Field of Search	Date
U.S. Class and subclass: 257/700,701,758,459,784,774,680,756,750,734,751,760,762,E23.02,E23.145,E21.582,E21.576	9/30/05 4/5/06
Other Documentation: foreign patents and literature in 257//700,701,758,459,784,774,680,756,750,734,751,760,762,E23.02,E23.145,E21.582,E21.576	9/30/05 4/5/06
Electronic data base(s): U.S. Patents EAST	9/30/05 4/5/06

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alexander O Williams
Primary Examiner
Art Unit 2826

AOW
4/5/06